Amendments to the Specification:

In the title:

METHOD FOR EXECUTING PATCH PROGRAM SEGMENTS AND ~~ENABLING A BRANCH CONTROL SYSTEM IN A MICROCOMPUTER~~ MICROPROCESSOR APPARATUS THEREOF

In paragraph [00012]:

The invention relates to a branch-control system for ~~systemfor~~ a microcomputer apparatus and more particularly, to a branch-control system for a ROM-programmed microcomputer apparatus.

In paragraph [0013]:

The prior art accomplishes the task of having the processing unit run a patch in lieu of a section of unwanted code in a ROM but not without disadvantages. The first prior art has too much overhead i.e. one marker bit has to be stored for each instruction in the ROM 12. If the program in the ROM 12 is very small, this may not be much of a disadvantage. However, as the size of the program in the ROM 12 becomes larger, the size of the corresponding the marker bit memory 26 becomes larger too. A larger size means a larger silicon die is needed to manufacture the chip, ~~chip,~~ which leads to increased production cost. Even if the marker bit memory 26 of the program patching module 20 were of small size, it is highly unlikely that one would need to branch off at every instruction in the ROM 12. Consequently, many of the marker bits would be of a value of 0 and therefore, wasted.

In paragraph [0017]:

According to the claimed invention, a microprocessor apparatus is disclosed. The

microprocessor apparatus comprises a ~~comprisesa~~ program counter for storing a program count value; a processing unit coupled to the program counter; a read only memory coupled to the processing unit for storing a first ~~afirst~~ program; an auxiliary programmable-memory coupled to the processing unit for storing patches to replace corresponding instructions in the first program along with a table containing a replacement program count value for each ~~foreach~~ patch; and a ~~anda~~ controller coupled to the program counter and the processing ~~the processing~~ unit for passing an indirect branch instruction corresponding to one of the patches to the processing unit in response to a match between the program count value and an initializing ~~aninitializing~~ program count value, wherein the indirect branch instruction will insert the replacement program count value corresponding to the match into the program counter. The aforementioned processing unit comprises an instruction fetching means coupled to the program counter for reading program instructions according to the program count value and storing fetched instructions in a buffer and an instruction decoding means coupled to the instruction fetching means for decoding and dispatching buffered instructions for execution.

In paragraph [0049]:

In contrast to the prior art, the ~~present~~ invention can implement a branching system using a controller 60 along with a table stored on an auxiliary memory 58 ~~memory58~~ so that the amount of hardware and cost is minimal. As can be readily seen, only one controller 60 with one register 62 is needed to accomplish one branch. For comparison, assume a ROM has 512 instruction lines and we would like to implement one branch at instruction 31 and replace it with instruction 831 in a patch on some other memory.